Analysis and optimization of Planar Rectangular 'I'-anode Schottky Barrier Diodes for Sulmillimeter-wave Multipliers

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Abstract

We report on the circuit modeling and analysis of a planar rectangular anode Schottky barrier diode "T-anode" to predict multiplier performance using these devices and to optimize their design. A rectangular anode Schottky barrier diode model, including sat urat ion effect, has been developed and implemented in Hewlet t Packard's Microwave Design System (MIX). This model, based on the diode geometry and semiconductor wafer structure, is used to optimize physical parameters such as the doping, epilayer thickness and anode size and shape in order to obtain maximum conversion efficiency. Different multiplier configurations (single and multiple diode doubler and quadrupler) to 640 GHz arc. analyzed and compared.

Introduction

In preparat ion for the instrument announcement of opportunist y for the Far Infrared and Submillimeter Space Telescope, an ESA/NASA space astrophysics observatory mission, local oscillator sources at high frequencies (1200 GHz) are being developed. As part of a multiplier chain beginning at -100 GHz, we are developing single and multiple-diode waveguide circuits up to 640 GHz. These multipliers are expected to have high efficiency and broad fixed-tuned bandwidth. Because of its proven performance. in this frequency range, the Schottky barrier diode is the nonlinear clement of choice for these multipliers. This paper considers the analysis and computed performance of new planar T-anode Schottky barrier diodes for use in multipliers from 200 to 1200 GHz. The planar circuit technology we are developing allows the incorporation of several diodes on the. same chip to increase the power handling, and/or to gang several multiplier stages together in a single waveguide mount. Optimum diode characteristics for given input frequency, power level and multiplier configuration are deduced.

Diode Model

The T-anode integrated planar Schottky barrier diode was developed at JPL for oscillator [1] and later for mixer [2],[3] applications. Recently we have begun employing these diodes in multiplier circuits. More than 8.5 mW and 15% efficiency have been obtained in a doubler to 270 GHz using these devices[4]. The excellent performance of the T-anode devices is attributed to the very low parasitic capacitance [5], as well as to their lower-than-average series resistance compared to traditional planar varactors. In order to take full advantage of these characteristics for multiplication up to 640 GHz, we have optimized, through computer simulations, both the anode geometry and device physical characteristics (doping, epilayer thickness, etc...) for different input power level and operating frequency.

With classical circular anodes contacted by an air bridge type finger, the parasitic become very important as the anode diameter is reduced (necessary for increased frequency operation), since the bridge width becomes larger than the diode diameter. The resulting overlap introduces a large parasitic capacitance between the finger tip and the active epilayer region surrounding the anode. Using the characteristic T-shaped cross section found on transistor gate circuits for the finger reduces these parasitic without increasing resistance in the bridge. The T gate geometry is shown Fig. 1. Measurement of the capacitance for two diodes of the same area, one with a circular anode and one with a rectangular T-anode, show substantially lower parasitic capacitance for the T-anode. structure. A measurement of a

typical anti-parallel-pair circular-anode Schottky diode with 1.5 μm^2 area yields 15 fF of total capacitance of which 6 . fF is contained in the junction and 9fF represents parasitic capacitance. For an anode of the same area but with the T cross section, wc measure a total capacitance of 9fF, of which 6 fF is in the junction and only 3 fF is parasitic. With this in mind we have proceeded to develop a numerical model for the rectangular T-anode structure.

The optimization are based on numerical analysis using Hewlett Packard's MDS, Momentum and HFSS programs [6]. An improved Schottky barrier diode model, including saturation effect [7], appropriate for the T-anode geometry, has been implemented in MDS. This model is based on the diode geometry and equivalent circuit shown in Fig. 1, and the non-linear diode model developed for the SPICE program [8]. The electrical parameters of the diode arc described as a function of the epilayer doping N_d, the epilayer thickness t_{epi}, and the anode dimensions L and W. Using the geometry shown in Fig.1 and the approach described in [9-12], wc can calculate the required diode electrical parameters.

R, as shown in Fig. 1, is the sum of the undepleted active layer (N-) resistance, the spreading resistance R_{spr} and the buried layer resistance R_{bl} in the N^+ layer, and the ohmic contact resistance R_{oc}. Using one section of the anode to calculate these resistances and integrating, we obtain:

$$R_e = \rho_{epi} \times \frac{t_{epi} - t}{W \times L} \qquad R_{spr} = \rho_{spr} \times \frac{W}{12 \times L}$$

$$R_{bl} = \rho_{bl} \times \frac{D}{2 \times L \times t_{bl}} \qquad R_{oc} = \frac{\sqrt{\rho_{cont} \times \rho_{bl}} / t_{bl}}{2 \times L}$$

where t_{epi} is the epilayer thickness, t, is the thickness of the depleted region, and is a function of voltage across the junction, $\rho_{epi} = 1 / N_d \times q \times \mu$ is the resistivity of the epilayer, t_{bl} is the thickness of the. buried layer, ρ_{bl} is the resistivity of the buried layer, ρ_{cont} is the resistivity of the ohmic contact, and ρ_{spr} is a weighted function of ρ_{epi} and ρ_{bl}. Finally

$$R_s = R_e + R_{spr} + R_{bl} + R_{oc}$$

This result leads to a second advantage of the rectangular T-anode Schottky barrier; reduced series resistance due to the rectangular rather than circular contact. For constant area, the calculated series resistance of a junction decreases when L increases and W decreases. This is shown Fig.2 for a 10 μm^2 anode. For comparison, R_s of a circular diode, with the same area is approximately 10 Ohms.

Using a classical approach to describe the non linear conductance and capacitance of the diode [8], we can complete the set of equations that are used in Ml)S. Once the parameters for the buried layer and the ohmic contact are set, this set of equations has four free parameters: the epilayer doping N_d, its thickness t_{epi}, and the diode dimensions L and W. t_{epi} is usually taken to be equal to t_{max}, the maximum value of the depletion layer before breakdown. In which case t_{epi} can be defined by N_d using (he depletion approximation:

$$t_{epi} = t_{max} = \sqrt{\frac{2 \times \varepsilon \times (\phi_{bi} - V_{br})}{q \times N_d}}$$

where V_{br} is the breakdown voltage, itself a function of N_d. The final model is then determined by N_d, L and W *only*.

An important consideration for varactor diode models is the current saturation effect. 'l'he limitation on varactor multiplier performance due to these effects has been shown by several authors. Kolberg et al. have shown that saturation is duc to carrier velocity limitation in the epilayer and have proposed an empirical model for this effect [7]. We have used their analysis, to limit our junction current by the value of the saturation current in our diode model :

$$i_{sat} = N_d \times v_{e.max} \times q \times L \times W$$

where $v_{e.max}$ is the maximum electron velocity in the epilayer, and is equal to 2,2x105 m/s in GaAs [7].

The model does not include inertia inductance. or displacement capacitance [9] (in order to reduce computing time) since they are second order. Parasitic duc to the geometric structure of the planar '1"-anode such as pad-pad and finger-pwl capacitance, air bridge inductance etc. could not be modeled accurately with lumped elements, instead we used the High Frequency Structure Simulator (HFSS) to compute the S parameters of a typical planar structure and have implemented it with our diode model in MDS. This completes our MDS electrical device. model.

Measured DC characteristics of actual devices show good agreement with those generated by the diode model, Fig. 3 shows a comparison of measured and modeled C(V). The modeled C(V) includes pad-pad and finger-pad capacitance, which shows that the parasitic duc to the anode contact are around 3 fF at O bias. R_s measurements for some T-anodes is as low as 6.1 Ohms for a 1.3x 10 μm^2 anode (N_d= 1 x 10^{23} m^{-3}, t_{epi}=.44 pm), for which our model predicts 635 Ohms.

Diode Opt imization

The diode model described above has been implemented in M DS in a multiplier circuit with ideal fi lters and matching impedances at each harmonic. This general multiplier model in MDS allows us to optimize any diode, or association of diodes, for any multiplication order. The. free parameters are L, W, and N_d for the diode and the different embedding impedances and bias voltage for the circuit, at a given input power and frequency. N_d is the most important parameter since its value is going to determine the limitation of the diode as a multiplier. A high value of N_d will decrease current saturation, but will reduce the breakdown voltage, thus reducing the voltage swing capability and the power handling capability of the diode. On the other hand, a low doping provides a high breakdown for high voltage swing, but increases the current saturation effect. It is obvious that a trade.-off must be made. Fig. 4 shows optimum efficiency for a doubler to 320 GHz and a single diode quadrupler to 640 GHz. The optimum value for N_d is apparent. A similar trade-off has to be made between R, and C_{j0}, therefore on the anode area LxW. To keep the length and width realizable, we limited W to a minimum value of 1 μm and 1, to a maximum value of 10 μm for these simulations. Hence, a 20 μm^2 diode would be 2x 10 μm^2, and not 1 x20 or .5x40, which would give better simulated performance duc to the lower series resistance, but would be very difficult to fabricate.

With the aid of our MDS model the optimum device and circuit parameters for a wide variety of multiplier configurations can be found. Charts such as those in Fig. 5 can be readily generated. Input power and frequency can be swept and physical device characteristics generated as shown. This simulation also gives the maximum output power one can expect for a given input power and frequency. Such charts can be computed for higher order multipliers, or for multipliers using multiple diode configurations (such as a balanced doubler, tripler with anti-series diodes, etc.. .).

640 GHz Multiplier Design

Since our primary goal was to design a multiplier to 640 GHz, it was important to determine which configuration would provide the best performance. within the fabrication constraints. Referring to Fig. 6, one can compare the performance of different multiplier configurations to 640 GHz at a specific input frequency and power. For example, one question commonly asked is whether to use higher order multiplication from a single device or chained multiplier stages. We compared the performance of an optimized quad rupler to 640 GHz, with two individually optimized and then cascaded doublers, and with a single two-stage doubler (two doublers on the same semiconductor chip, with the same epilayer and doping for all devices). The comparison was performed with 15mW input power at 160 GHz. We also compared the performance of circuits with one and two diodes in series, using realistic circuit limitations. in this comparison, the anode geometry, as well as the epilayer doping and thickness and the circuit embedding impedances (limited to a realistic range) have been optimized. The simulations show the benefit of multiple device configurations, since two diodes in series distribute the. voltage swing, and allow a higher doping to

reduce saturation effect. Fig. 6 illustrates the trade-offs between performance and complexity to obtain optimum pert'ormance at 640 GHz.

As a first step towards realizing a 640 GHz source. we have chosen to develop a quadrupler to 640 GHz with 1 diode, as well as two doublers, one to 320 GHz, the second to 640 GHz using the first as input. To reduce cost and fabrication time, they are all fabricated on the same wafer, which has a doping of $3x10^{23} m^{-3}$, and is therefore not optimum for each individual multiplier (but will be for a two device quadrupler). With the doping fixed, we have optimized diode dimensions for best performance. The computed results for 15 mW input at 160 GHz are: 1.8 mW for the chained doublers (12.5% overall efficiency), and 0.7 mW (4%) for the quadruple. The all-planar circuits have been designed [13], and will be measured soon. A design for a quadruple with two diodes in series (P_{out}=2.7 mW, efficiency=18%) is in preparation.

Conclusion

A versatile circuit model has been developed for the T-anode Schottky varactor diode and implemented in HP MDS. "l'his model allows detailed predictions of multiplier performance at any submillimeter wavelength and can be used to optimize both device and circuit characteristics. As an example, the model has been used to compare the performance of single and multiple diode doublers and quadruplers for 640 GHz. It remains to be. seen how accurate these performance predictions are. Fabrication of the optimized circuits is now ongoing and will be the subject of a later paper.

Acknowledgments

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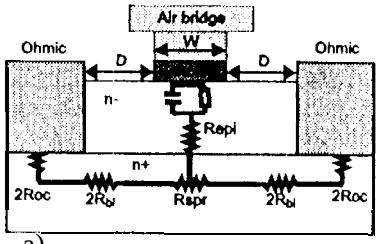
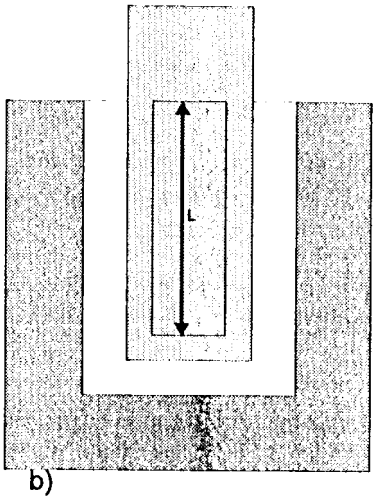
Figures



a)



b)

c)

Figure 1- Geometry of the l-anode Schottky diode, used to describe the voltage dcpcndcnt conductance and capacitance, as well as parasitics and saturation. a) cross section of the l'-anodc, b) top view of the rectangular T-anode junction, c) SEM picture of a T-anode diode.

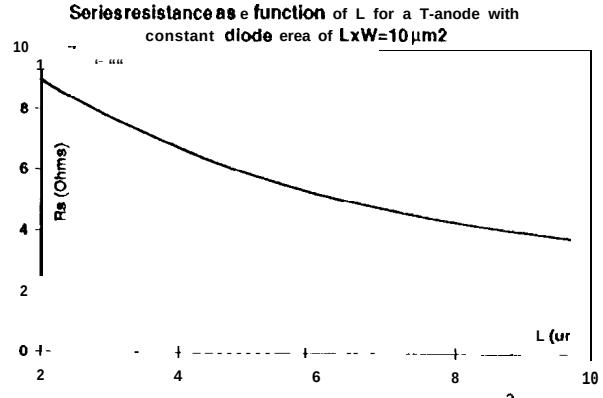


Figure 2-R_s versus L for a T-anode with 10 μm^2 area.

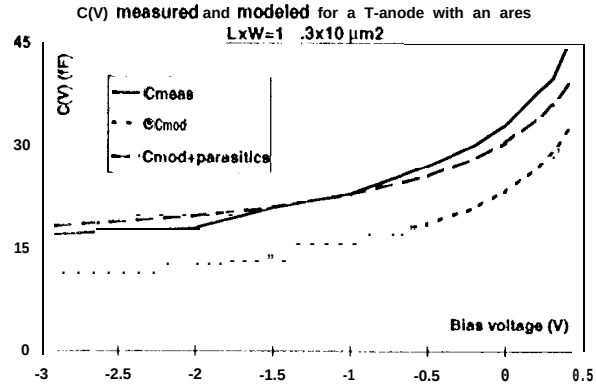


Figure 3-C(V) measured and modeled, with and without parasitic, for a 13μm^2 '1'-anodc,

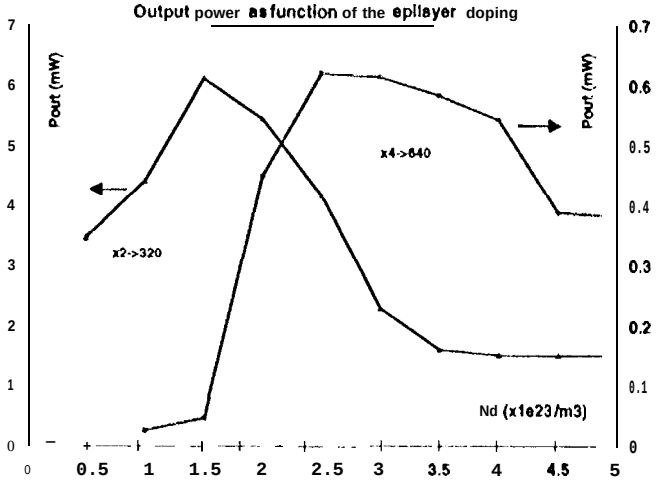


Figure 4- Predicted Output power for a doubler to 320 GHz, and a quadrupler to 640 GHz, as a function of epilayer doping. For each point, embedding impedances, bias and anode dimensions are optimized.

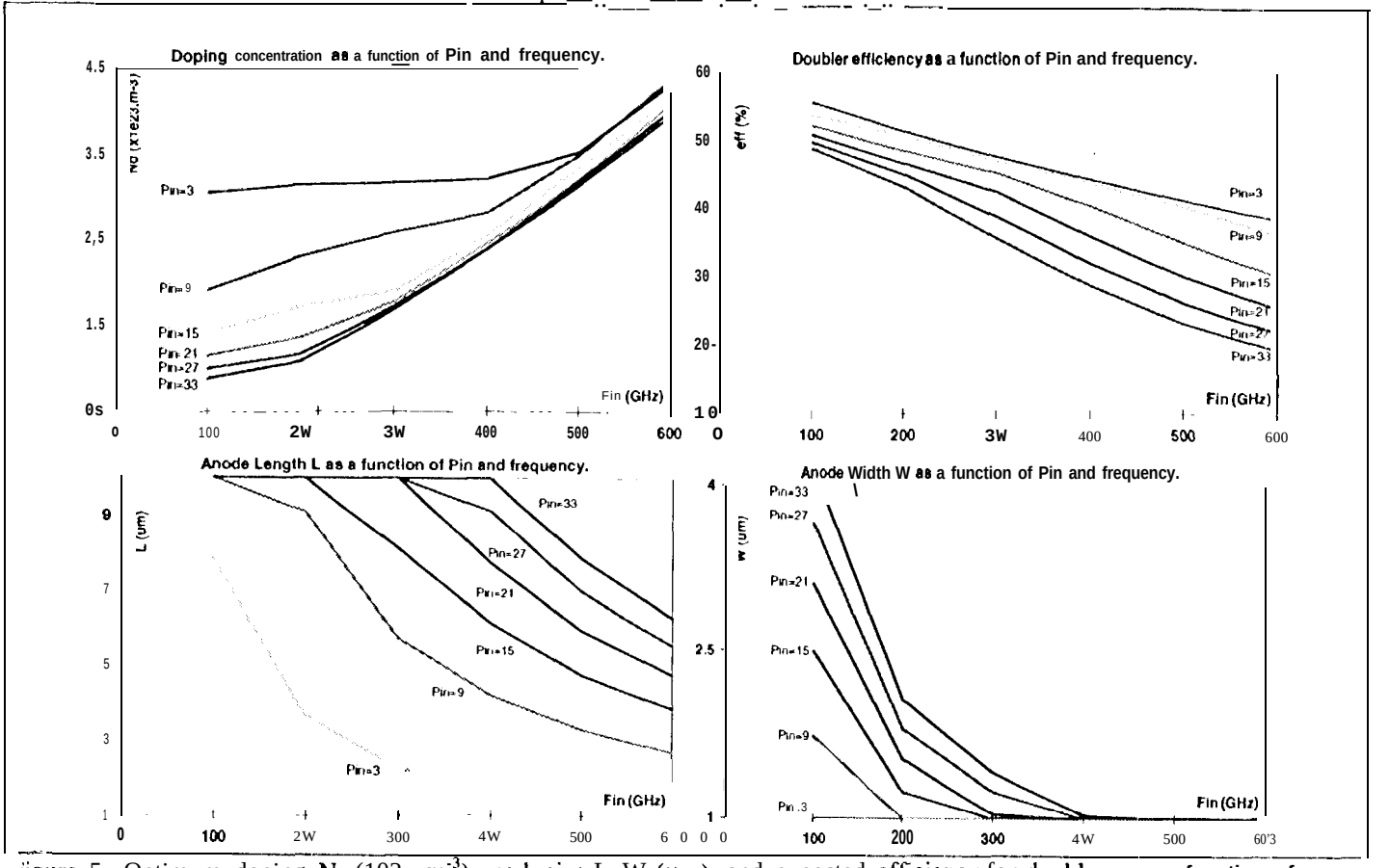


Figure 5- Optimum doping N_d (102~ m^{-3}), anode size LxW (μm), and expected efficiency for doublers, as a function of input frequency (100 to 600 GHz), and power (3 mW to 33 mW). All results are for optimum embedding impedances. The anode dimensions (I, and W) are limited between 1 and 10 μm.

multiplier type	Anode limitations: Lmax=10um Wmin=1um	
'two 1 diode chained doublers, same doping	Pout=1.9 mw A1=10*1 A2=3*1	eff=12.5% Nd1=3.3
two 1-diode chained doublers, two dopings	Pout=2.3mW A1=10*1.2 A2=3.5*1	eff=1 5.3% Nd1=1.6 Nd2=3.7
two 2-diode chained doublers, same doping	Pout=3.9mW A1=8*1 A2=2.5*1	eff=26% Nd1=3.5
Quadrupler with 2 diodes in series	Pout=2.7 mW A1=7.5*1	eff=18% Nd1=3
Quadrupler with 3 diodes in series	Pout=4.1mW A1=6.5*1	eff=27% Nd1=3.4

Figure 6- Comparison of performance for different multiplier configurations to 640 GHz with 15 mW input power. Each configuration is shown with different diode dimension limitations. Shown are the optimized performance, doping and anode dimensions. A 1, A2 are diode areas (LxW in microns), Nd 1, Nd2 are epilayer dopings xl $0^{23}/m^3$.